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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/384,504	08/27/1999	JOHN W. MARSHALL	112025-0166	7925

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CESARI AND MCKENNA, LLP  
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EXAMINER

BRODA, SAMUEL

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/384,504

Applicant(s)

MARSHALL ET AL.

Examiner

Samuel Broda

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 August 1999.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 August 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All   b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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### DETAILED ACTION

1. Claims 1-12 have been examined.

#### *Drawings*

2. The Draftsperson has objected to the drawings; see the copy of Form PTO-948 for an explanation.

#### *Claim Rejections - 35 U.S.C. § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

...

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.1 Claims 1-12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by McDonald et al, "Timing Analysis for the PA-8000", EE Design, February 1997 (downloaded text from: [www.eedesign.com/editorial/1997/coverstory9702.html](http://www.eedesign.com/editorial/1997/coverstory9702.html)).

3.2 Regarding claims 1-12, McDonald teaches the use of the "PathMill" timing simulator along with a hierarchical analysis of RC networks and includes generation of 'gray box' and 'minichip' block abstractions that contain a physically accurate description of latches and blocks, with circuit models having "an integration of gray boxes, transistors, and RC parasitics. This flexibility provides an elegant structure for timing verification of hierarchical designs." Text download, page 7 paragraph 4; see generally text download pages 6-8.

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### *Conclusion*

4. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure. Reference to Rodriguez-Garcia, "A Tool for Complete Small-Signal Analytical Modeling of Large Analog Circuits", IEEE Third International Workshop on Design of Mixed-Mode Integrated Circuits and Applications, pp. 36-39 (July 1999), is cited as teaching hierarchical analysis techniques applied to symbolic analysis.

Reference to Tan et al, "Balanced Multi-Level Multi-Way Partitioning of Large Analog Circuits for Hierarchical Symbolic Analysis", IEEE Proceedings of the Asia and South Pacific Design Automation Conference, Vol. 1, pp. 1-4 (January 1999), is cited multi-way partitioning used in performing hierarchical symbolic analysis.

Reference to Shepard et al, "Design Methodology for the S/390 Parallel Enterprise Server G4 Microprocessors", IBM Journal of Research and Development, Vol. 41 No. 4/5, pp. 515-547 (July 1997), is cited as teaching performing a hierarchical analysis as part of a power estimation using the SPECS simulator combined with a defined set of "power points." See pages 540-541.

5. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (703) 305-1026. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

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If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:

(703) 746-7238 --- for communications after a Final Rejection has been made;

(703) 746-7239 --- for other official communications; and

(703) 746-7240 --- for non-official or draft communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.



SAMUEL BRODA, ESQ.  
PATENT EXAMINER